# Three-Dimensional Passive Circuit Technology For Ultra-Compact MMIC's

Makoto Hirano, Kenjiro Nishikawa, Ichihiko Toyoda, Shinji Aoyama, Suehiro Sugitani, and Kimiyoshi Yamasaki

*Abstract*—**A novel passive circuit technology of a three-dimensional (3-D) metal-insulator structure is developed for ultra-compact MMIC's. By combining vertical passive elements, such as a wall-like microwire for shielding or coupling, and a pillar-like via connection with multilayer passive circuits, a 3-D passive circuit structure is formed to implement highly dense and more functional MMIC's.** $O_2/He$ **RIE for forming trenches and holes in a thick plyimide insulator, low-current electroplating for foming gold metal sidewalls in the trenches or holes, and ion-milling with a WSiN stopper layer for patterning the gold metal are used to produce such a structure. The complete 3-D structure provides miniature microstrip lines effectively shielded with a vertical metal-wall, a miniature balun with low-loss vertical wall-like microwires, and inverted microstrip lines jointed with pillar-like vias through a thick polyimide layer. This technology stages next-generation ultra-compact MMIC's by producing various functional passive circuits in a very small area.**

## I. Introduction

RECENT RAPID improvement in mobile communication has increased demand for highly dense and more functional MMIC's. A multilayer passive circuit with polyimide insulator is one useful approach for such MMIC's [1]–[3]. As shown in Fig. 1(a), two different passive circuits can be formed in the same area with a shield ground plane in the middle metal layer, and moreover, two or more different signal lines can be coupled throughout a window formed in the shield plane. Therefore, by using this technology, miniature dividers, couplers, mixers or many other functional passive circuits have been designed.

On the other hand, vertical microwire technology [4], [5] is another effective devise for shrinking the size of MMIC's. As shown in Fig. 1(b), inductors and transmission lines can be miniaturized by a vertical wall-like microwire structure. About one-third to one-fourth miniaturized inductors or transmission lines have been obtained by this technology. If we can combine these two technologies, and add some more advanced features, denser and more highly functional MMIC's will be implemented.

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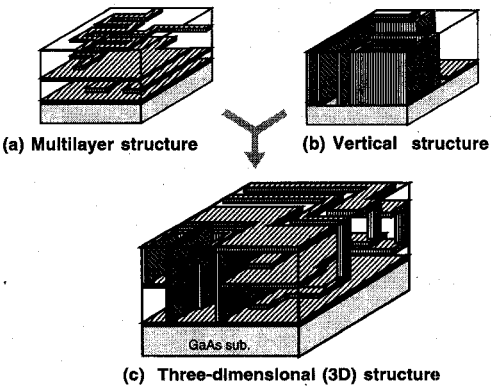



Fig. 1. The structure of compact MMIC's.

In this paper, a novel passive circuit technology for more compact and functional MMIC's is proposed. For staging such next-generation MMIC's, a vertical passive structure and multilayer one are combined in completely three-dementionalized (3-D) passive structure. As a result, circuit designers can take advantage of smaller chip area and get higher performance and greater design frexibility of MMIC's.

## II. A Structure

The most desirable structure to advance passive functions of MMIC's is a completely three-dimensional one, which consists of vertical metal structure and multilayer metal-insulator structure, both buried in a thick insulator. In such a structure, many vertical passive elements can be utilized to design MMIC's; a vertical shield wall, a miniature inductor, a miniature transmission line, a vertical coupler and a pillar-like via connection through a thick insulator layer. In addition, all these elements can be put together with a horizontal multimetal layer, as shown in Fig. 1(c). Fig. 2 shows some examples of combining vertical elements and horizontal elements to make three basic 3-D passive components: a 3-D shield ground plane, coupled signal lines, and 3-D interconnections. By employing these basic 3-D components, a variety of passive functional circuits, such as divider, phase shifter, filter and so forth, can be formed to minimize the chip area and achieve greatly improve on the performance of MMIC's.

## III. Fabrication

In order to achieve a 3-D passive circuit structure, a new fabrication technology was developed. We call it folded metal

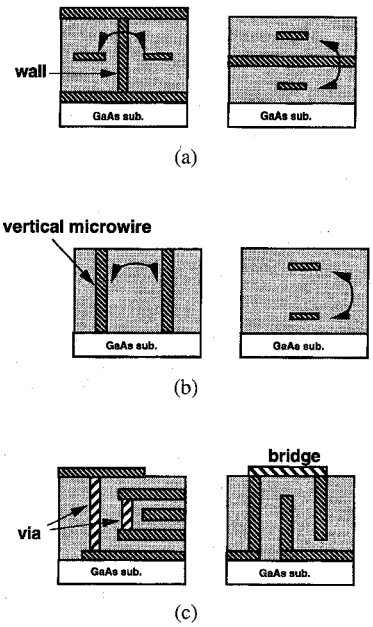



Fig. 2. Three basic effects in 3-D structure. (a) Shielding, (b) coupling, and (c) interconnecting.

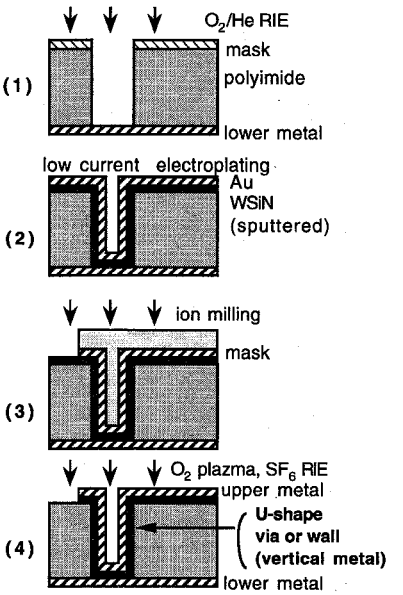



Fig. 3. Process flow of buried vertical $U$-shaped vias or walls.

interconnection technology with thick insulator (FMIT). In this technology, a $U$-shaped microwire [4], as an essential vertical element, is buried in a thick insulator of multi-metal-insulator-layer structure. The main flow of the fabrication process is shown in Fig. 3.

The process has three key features; First, via-holes and trenches are formed in a 10-$\mu$m-thick polyimide insulator layer by RIE. Second, a metal side-wall is formed along the surface of the formed holes and trenches. Finally, the gold grown on the polyimide surface is patterned. The detailed fabrication methods and conditions are as follows.

### A. $O_2$/He *RIE for Polyiomide Etching*

To form via-holes and trenches in the thick polyimide insulator layer, $O_2$/He RIE was used. To prevent large side-etching of polyimide, RIE was performed at low pressure, 30 mtorr. In etching for polyimide with thickness over 2 $\mu$m, some residue is produced on the bottom surface of the holes and the trenches by using $O_2$ RIE without He. To eliminate this residue, a mixture of $O_2$ and He was used in RIE. The cleaning effect of the bottom surface by adding He to $O_2$ RIE is shown in Fig. 4. In comparison with the bottom surface, formed by only $O_2$ RIE, that formed by the mixture gas RIE was cleaner. This cleaning effect is caused by the sputtering effect of He ions. Employing the etching condition of 30 mtorr gas pressure with a 2:1 combination of $O_2$ and He at 0.2 W/cm$^2$ RF power density, vertical holes and trenches were successfully formed without both large side-etching and etching residue.

### B. *Low-Current Electroplating for Gold Metal Sidewall*

To form the metal sidewall along the whole surface of the formed holes and trenches in the polyimide, low-current gold

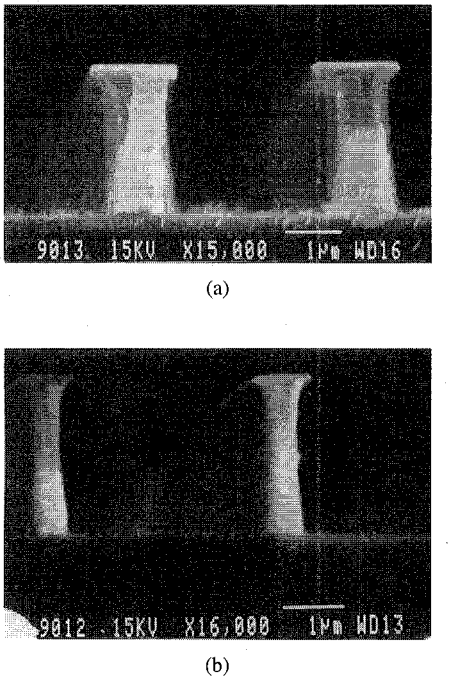



Fig. 4. SEM images of trenches formed in polyimide. (a) Trenches in a polyimide formed by $O_2$ RIE, and (b) trenches in a polyimide formed by $O_2$He RIE.

electroplating was applied. By lowering the current density for plating, conformability and uniformity of a plated metal are improved [6].

Fig. 5 shows the relation of plating current density versus conformability and unformity of gold metal. As can be seen in this figure, the relative thickness of the sidewall in a trench and a standard deviation of sheet resistance of the plated gold in a wafer were both increased by lowering the current density, i.e., the plating rate of electroplating.

The crystal structure, with better microscopic uniformity, of the gold plated on the 50-nm-thick gold layer made by

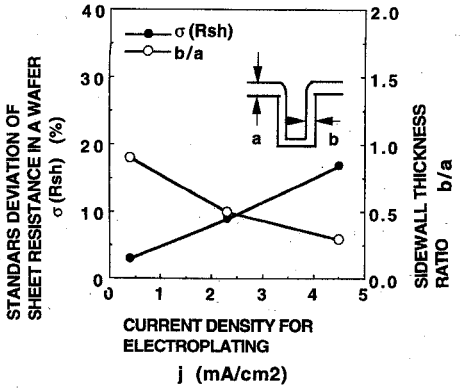



Fig. 5. Conformability of gold metal plated in trenches.

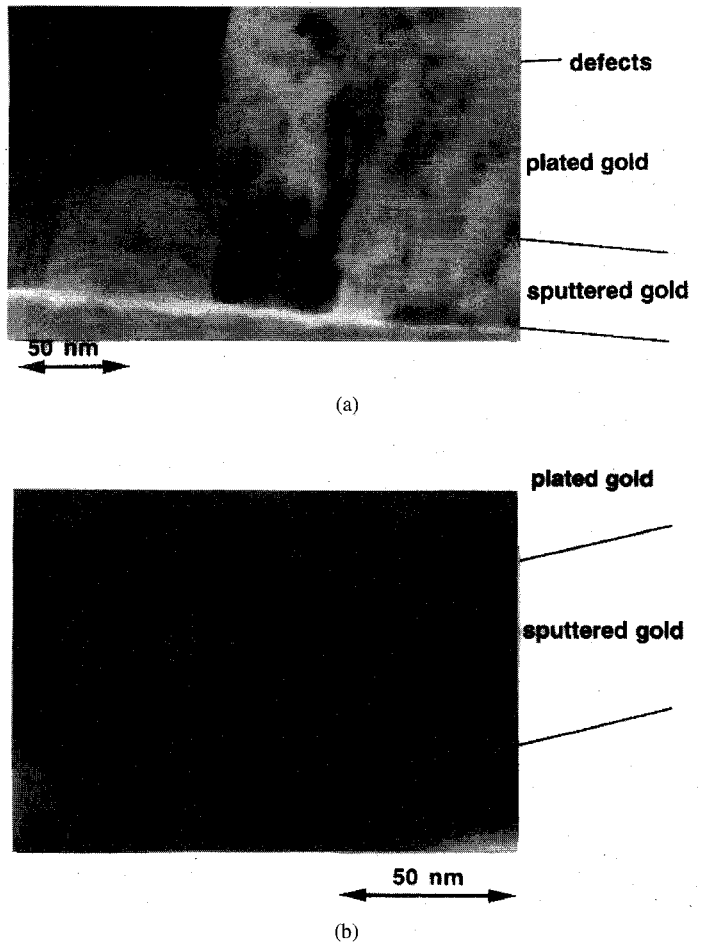



Fig. 6. TEM images of plated gold metal. (a) Gold metal plated by high current density, 3mA/cm2, and (b) gold metal plated by low current density, 0.2 mA/cm2.

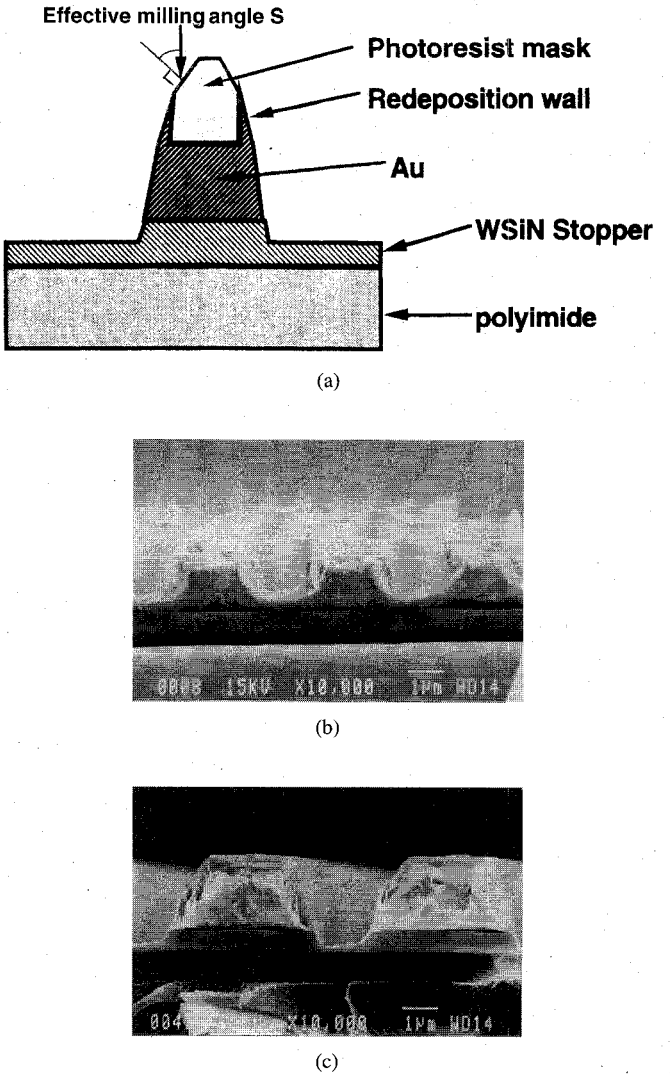


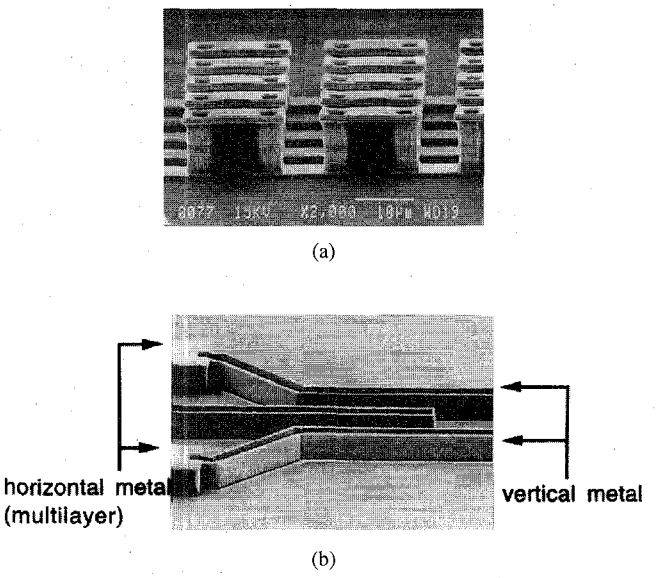

Fig. 7. Patterned gold metal by ion-milling. (a) Schematic view of Au patterning by ion-milling. (b) SEM image of formed pattern (using a mask photoresist with large thickness), and (c) SEM image of formed pattern (using a mask photoresist with optimized thickness).

sputtering deposition was also studied by TEM. Fig. 6(a) shows the grain size and defects in the metal plated by a large current density, 3 $mA/cm^2$, and Fig. 6(b) shows those in the metal plated by a small current density, 0.2 $mA/cm^2$. Larger grain size and less defects were obtained with the lower current density. The crystal structure obtained with the low current density will take advantage to achieve long lifetime of interconnection microwires by preventing electromigration. By using low-current plating conditions, with current density of 0.2 $mA/cm^2$, thick gold sidewalls as $U$-shaped vias and vertical microwires were successfully formed.

### *C. Ion-Milling with WSiN Metal Stopper*

To pattern gold grown on the whole surface, including holes and trenches, ion-milling is used with WSiN metal as a stopper. The stopper metal protects the lower polyimide from ion-milling and also from etching when the photoresist as a milling-mask is removed by $O_2$ plasma. The WSiN layer with thickness of 200–400 nm beneath the gold was useful for patterning a 1-$\mu$m-thick gold layer in the 3-D structure.

The thickness of the photoresist mask for ion-milling is another key factor to get fine patterns of the gold metal. To prevent redeposition of gold onto the sidewall of the photoresist mask, which often produces electrical short error between upper and lower interconnections, the photoresist




(a)

(b)

Fig. 8. Fabricated vertical metal structures. (The polyimide has been removed to reveal the metal structure.) (a) Pillar-like vias (10 micron height), and (b) wall-like microwires (10 micron height).

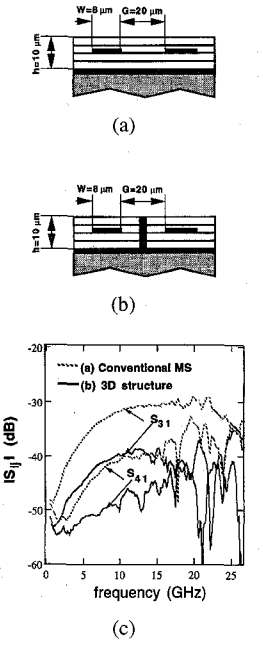



Fig. 9. Shielding effect of a vertical metal wall for microstrip (MS) lines. (a) Conventional MS (multilayer structure), (b) MS with shield wall (3-D structure), and (c) high frequency characteristics.

mask should be designed to become thin and tapered at the pattern edges at the end of ion-milling. The milling rate of the photoresist is larger at the pattern edge, i.e., the shoulder of the photoresist, than at the pattern center (shown in Fig. 7(a)) because of the milling rate dependency on the Ar incidented angle. Therefore, the optimum thickness of photoresist mask can be designed by the following equation

$$T = tX dT' / \cos S$$

where, $T$ is thickness of the photoresist, $t$ is etching time including over-etching time for the gold metal, $dT'$ is the maxmum etching rate of the photoresist for an angled ion-beam, $S$ is the milling angle for maxmum etching rate.

A schematic of the cross section of the mask and the gold metal in the milling process and SEM images of gold patterns fabricated by two photoresist masks with different thickness are shown in Fig. 7(a)–(c). As shown in the Fig. 7(c), the fine gold patterns were formed without redeposition-walls by optimizing the thickness of the photoresist.

The 3-D passive structure with thickness of 10 $\mu$m, fabricated by using all the above-mentioned techniques is shown in Fig. 8(a) and (b). In the figures, the polyimide insulator was almost removed by RIE for SEM observation. The 10-$\mu$m-height pillar-like via and metal wall were successsfully fabricated. These can be combined with, for example, a multilayer of five 1.4-$\mu$m-thick metal layers and four 2.5-$\mu$m-thick insulator layers. In such a combined structure, the pillar-like via connections in the height range of 2.5–10 $\mu$m have been successfully fabricated with 100% yield in a 3-inch-diameter wafer. Even by only the combination of this vertical structure and the multilayer one, many varieties of miniature passive circuits can be formed on an IC chip as described in the following section.

## IV. Circuit Applications

Basic effects of 3-D structure have been confirmed as follows.

### A. Shield Effect with Vertical Structure

Fig. 9 shows one example of shielding effect with a vertical metal wall.

The isolation characteristics were compared for two structures; one with only two microstrip (MS) signal lines of multilayer structure being put in seperation (Fig. 9(a)), and the other being shielded with a vertical metal wall buried in the thick polyimide (Fig. 9(b)). As shown in Fig. 9(c), the lines can be shielded effectively employing the vertical metal wall. By using the shield effect with a vertical wall or a horizontal plane in the 3-D structure, thin film microstrip (TFMS) lines can offer a significantly reduced occupied area providing strongly isolated crossover.

### B. Miniature But Low-Loss Characteristics of the Vertical Wall-Like Microwires

Another 3-D passive circuit as an example of using miniature but low-loss vertical microwires, a one-third or less miniaturized wideband balun, has also been successfully operated [7]. A balun with 1.5 $\pm$ 1 dB insertion loss over 10–30 GHz and 2 dB and 5 degrees of amplitude and phase balances over 5–35 GHz have been obtained with the intrinsic area of only 450 $\mu$m $\times$ 800 $\mu$m. The detailed characteristics was described in [7]. By using the coupling effect with vertical or horizontal metals, many other functional passive circuits like dividers, filters and mixers can be fabricated in a small area.

### C. Vertical Pillar-Like Vias Through Thick Polyimide Insulator

Vertical connection by pillar like vias can provide short signal delay and miniaturized connection even through a very thick insulator. An inverted microstrip line (IMSL) with a thick insulator [8] has been successfully formed by this technology, which is useful not only for 3-D MMIC's but also for ultra-high-speed digital IC's.

The 3-D structure can also be used for many other passive elements such as low loss vertical inductors [4], miniature vertical co-planer transmission-lines [5], a multilayer coupler [2], [3] and microstrip lines shielded with a middle layer ground plane [2], [3]. The high-frequency characteristics of these 3-D elements have already been confirmed [2]–[5].

## V. Conclusion

Three-dimensional (3-D) passive circuits were successfully fabricated in 10-$\mu$m-thick polyimide insulator. A new fabrication technology, folded metal interconnection technology with thick insulator (FMIT), was developed to achieve the 3-D structure. By using this technology, vertical $U$-shape metal walls and vias were buried in the polyimide, which also contained horizontal metal layers. The structure provided miniature microstrip (MS) lines effectively shielded with a vertical wall, and a miniature balun consisted of low-loss vertical microwires. This technology could also provide inverted microstrip lines (IMSL) with a polyimide layer of over 10-mm-thickness. Because 3-D technology can achieve a variety of highly miniaturized and functional passive circuits, it enables us to implement ultra-compact MMIC's.

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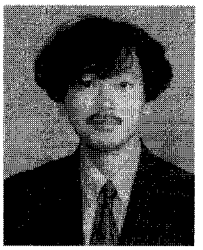

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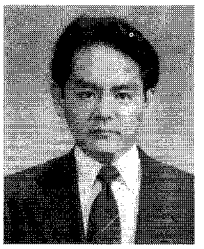

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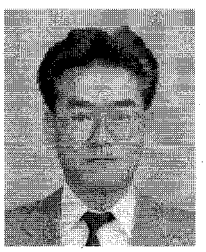

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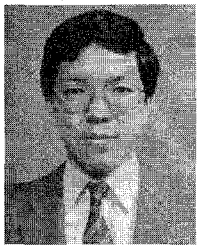

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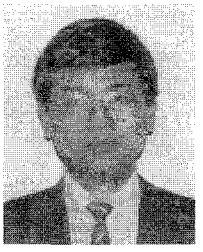

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